

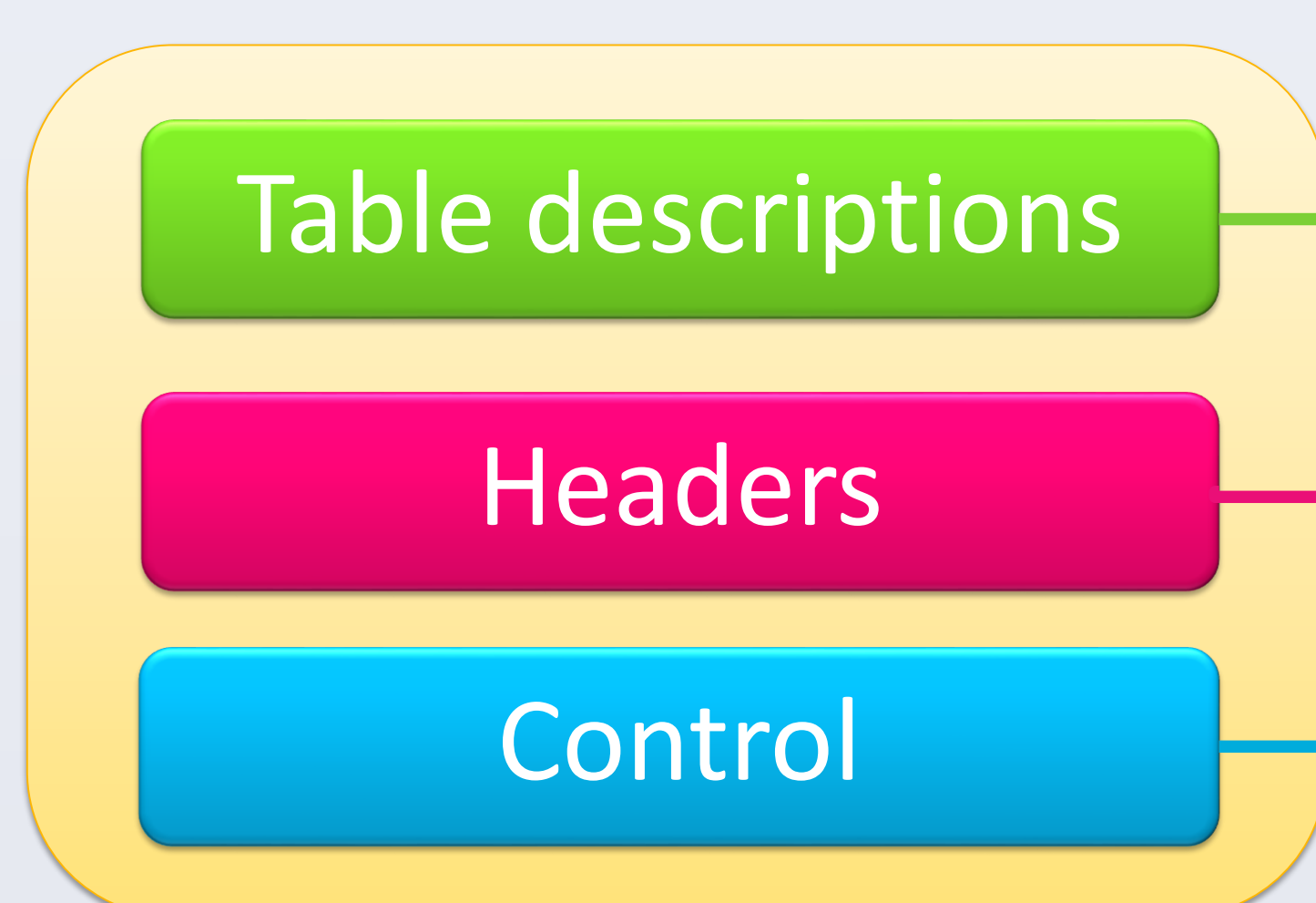
High speed packet forwarding compiled from protocol independent data plane specifications

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P4

P4 is a high level language for programming packet processors, enabling great flexibility in the description of packet structure and processing, independent of the specifics of underlying hardware. P4 works in conjunction with SDN control protocols like OpenFlow.

P4 program

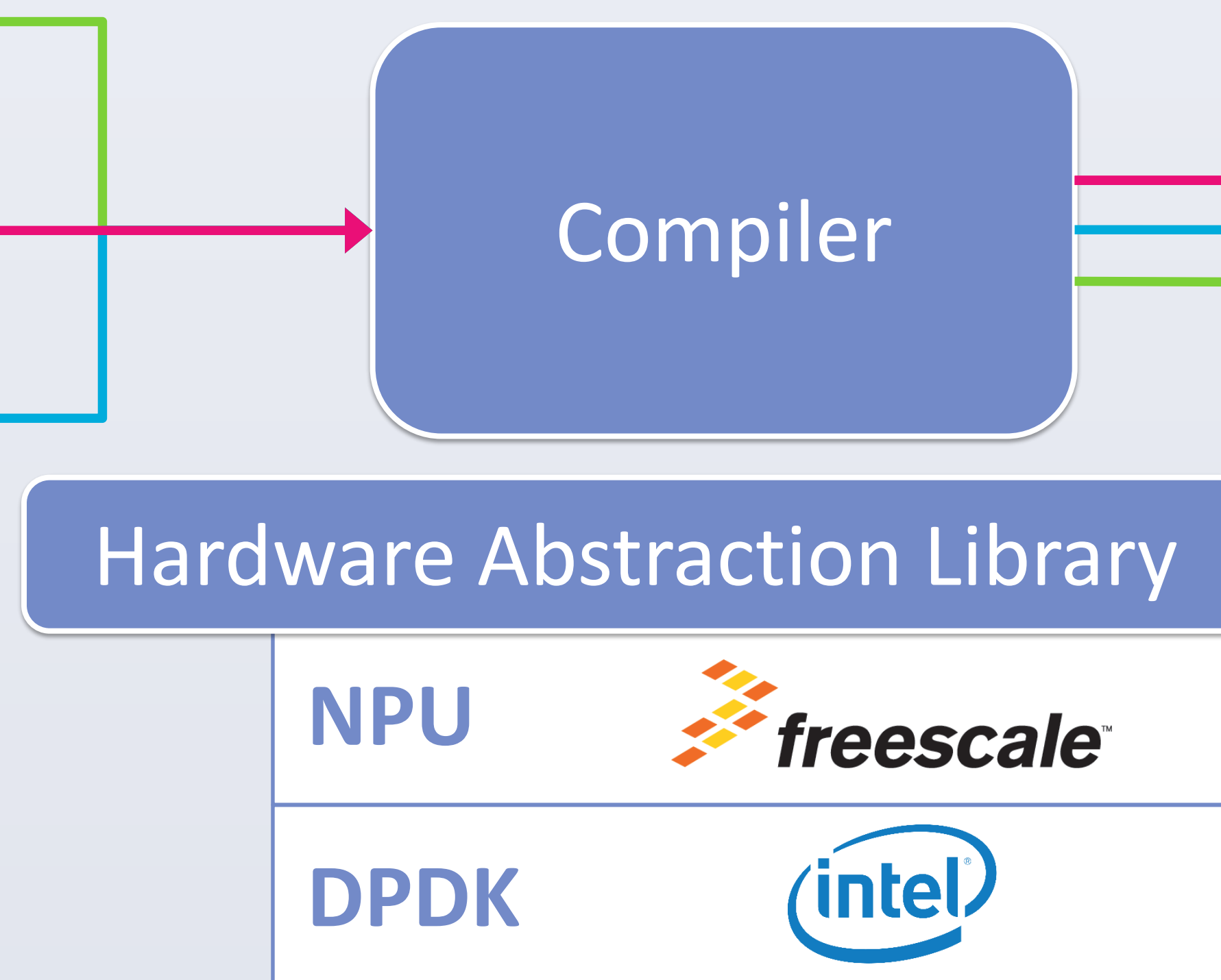


Compiler

Our retargetable compiler turns a P4 code into a target independent core program running on the top of a Hardware Abstraction Library.

HAL

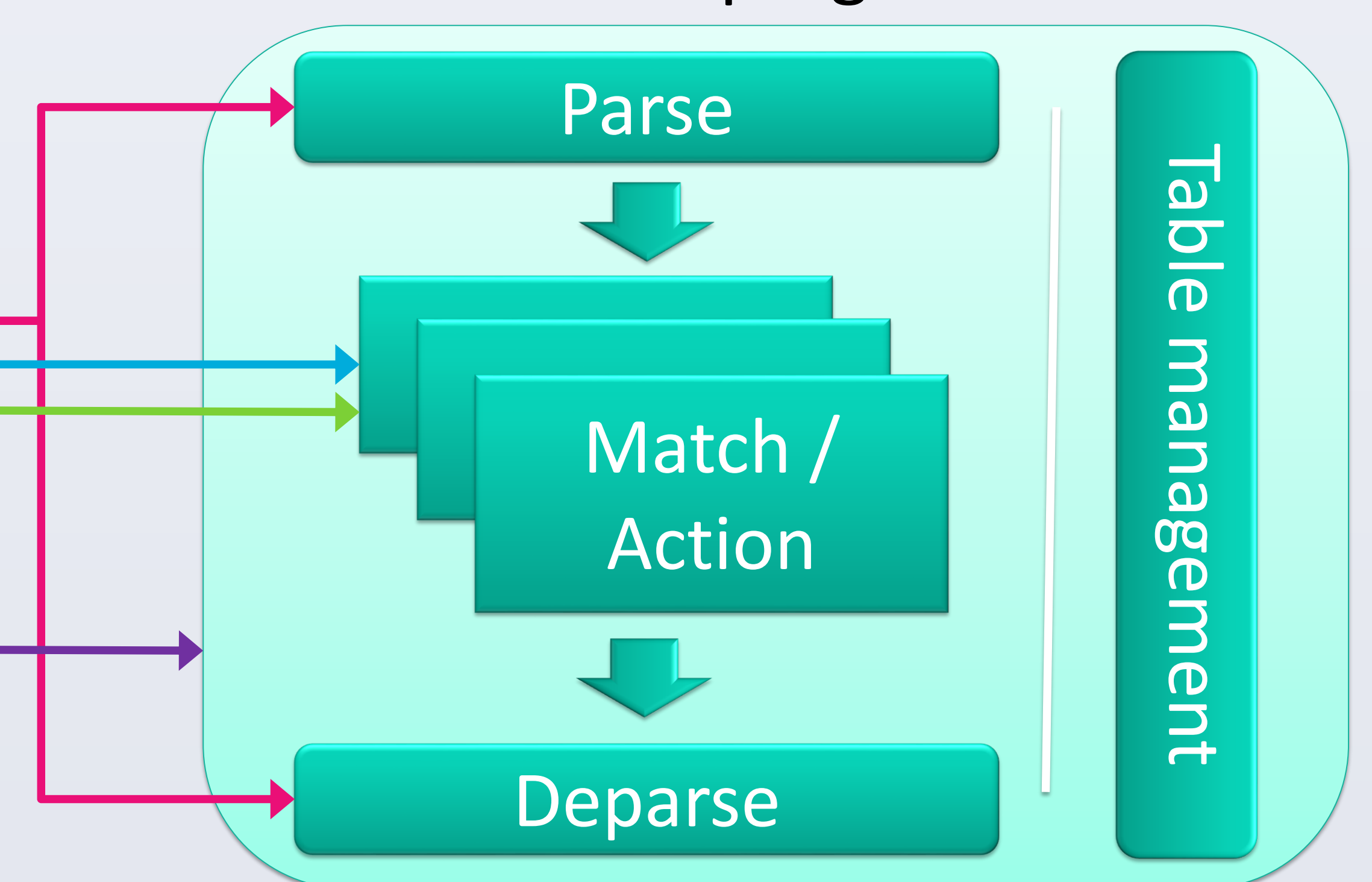
Hardware dependent operations are separated to the Hardware Abstraction Library (HAL) which improves portability: to support a new architecture, only a new HAL needs to be implemented.



Switch program

To run the core program on a specific hardware the appropriate HAL needs to be linked. The compiled switch program then parse incoming packets, apply match-action rules and deparse messages before egressing.

Switch program



OBJECTIVES

- Retargetable P4 compiler
- High performance packet processing
- Reconfigurable
- Modular switch program

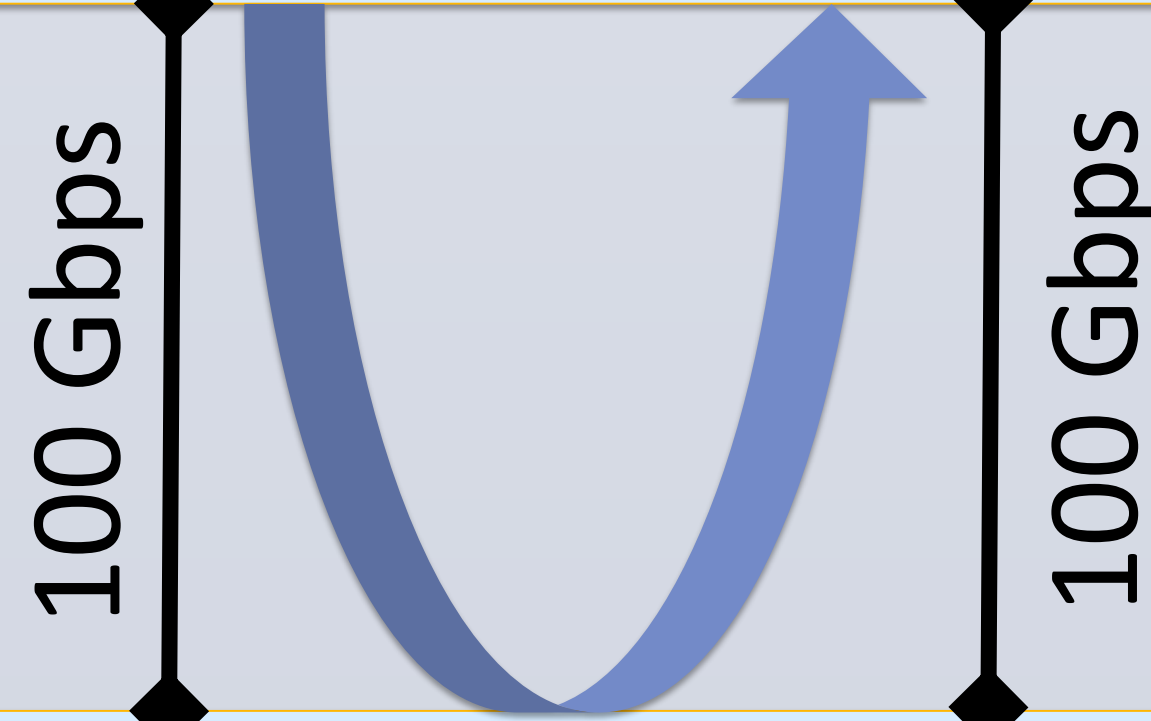
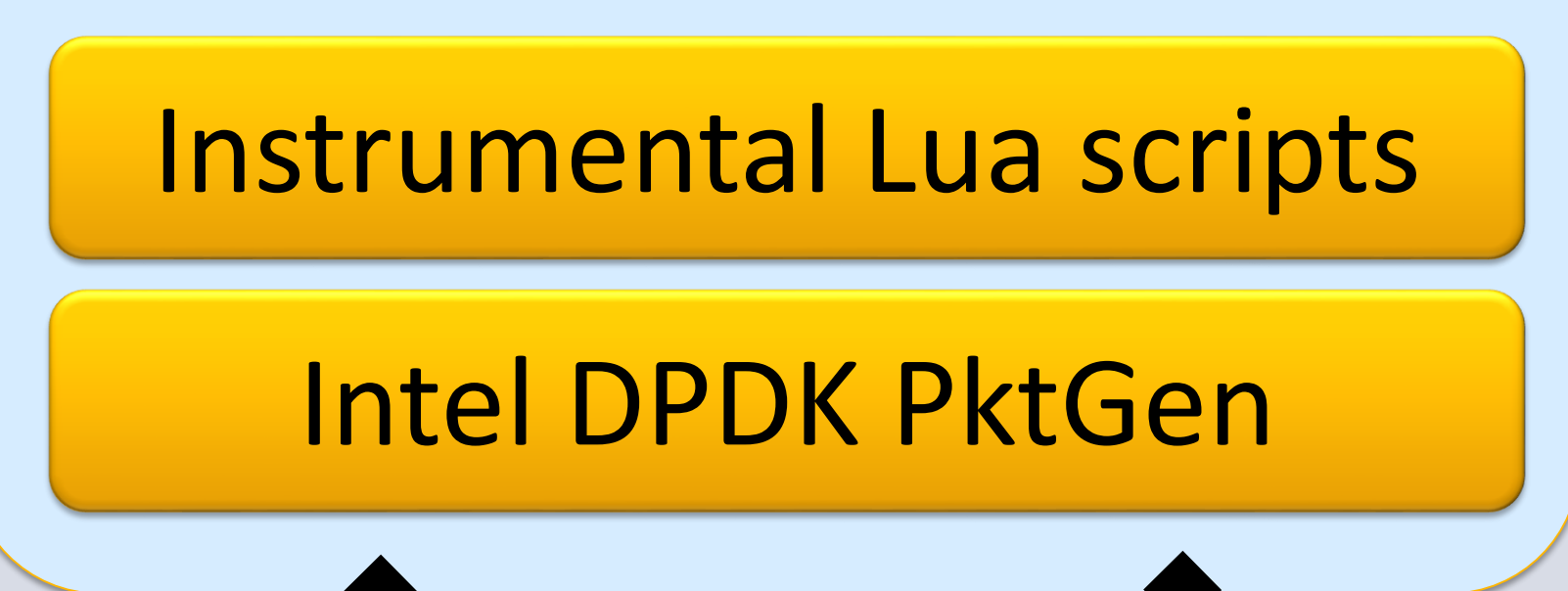
EVALUATION

- L2 forwarding with MAC learning via digest generation
- Demo controller fills tables smac and dmac
- Mellanox ConnectX®-4 100Gb ethernet cards
- 1x100Gbps pseudo realistic test traffic (random mac and IPv4 addresses and TCP ports)

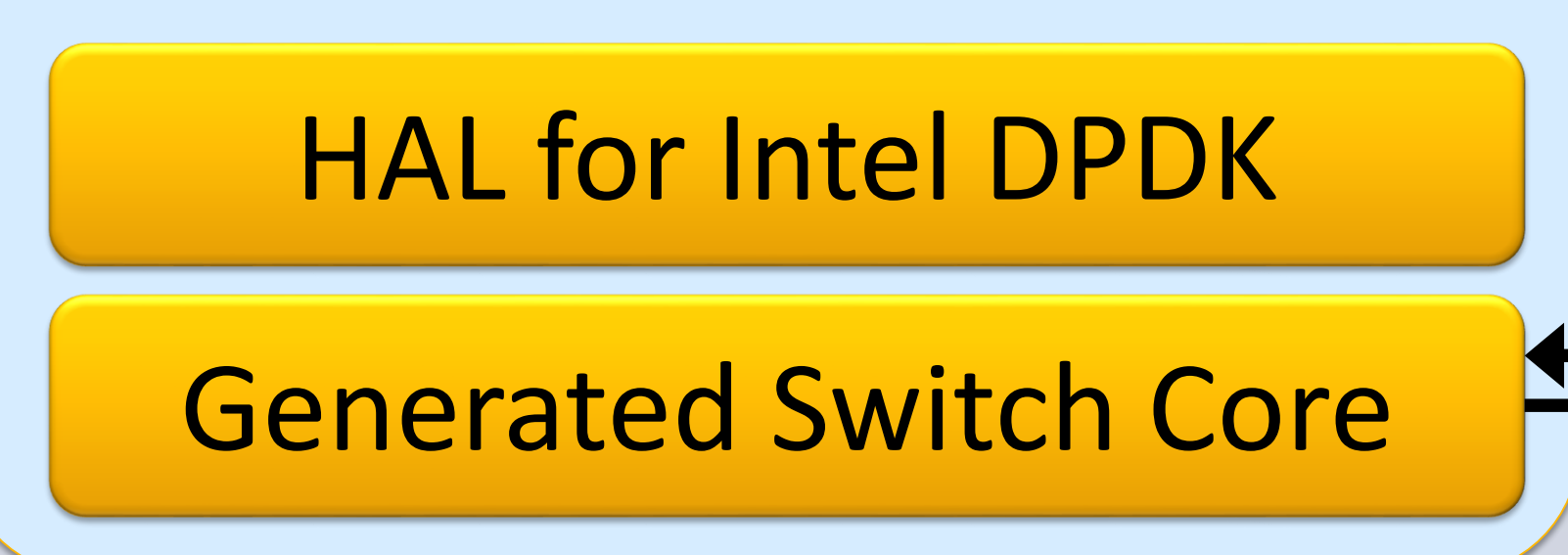
RESULTS

- Almost complete P4-14 compiler with HAL for Intel DPK
- NUMA support
- Run-to-completion model
- Comparable performance to official DPK implementations
- Working L2/L3 switch examples
- Other HALs are coming soon

TrafficGen Node



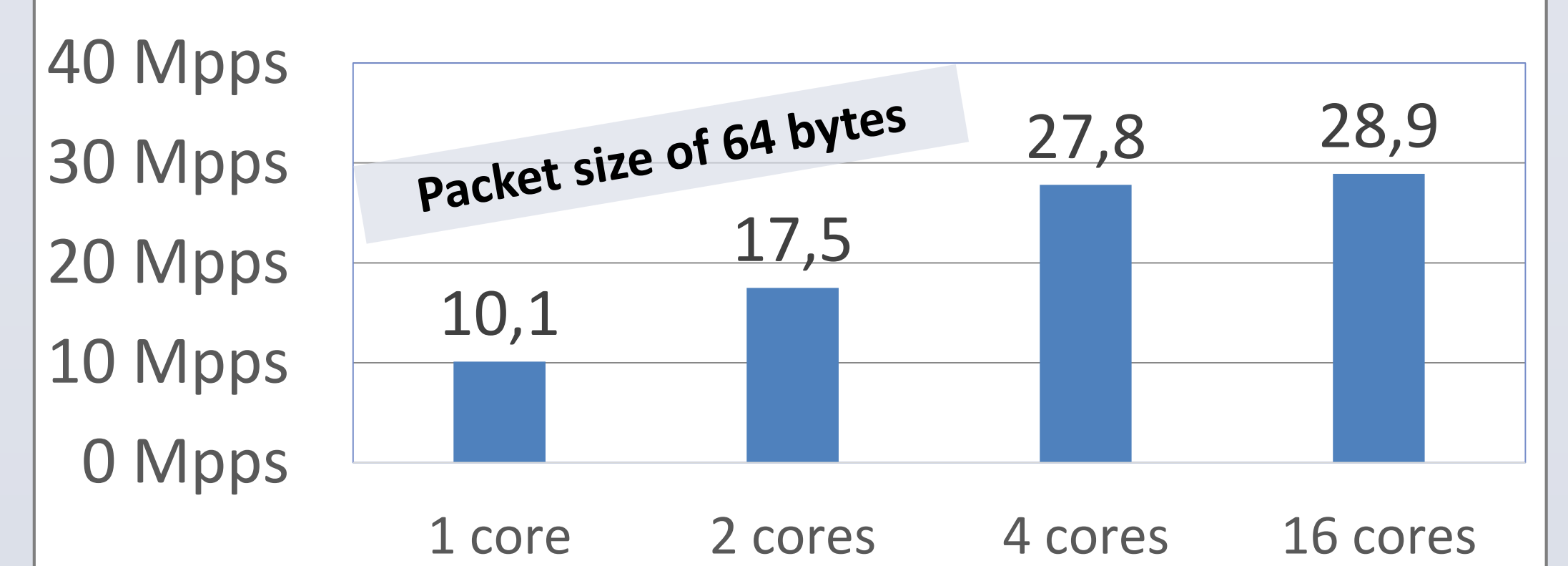
P4Switch Node



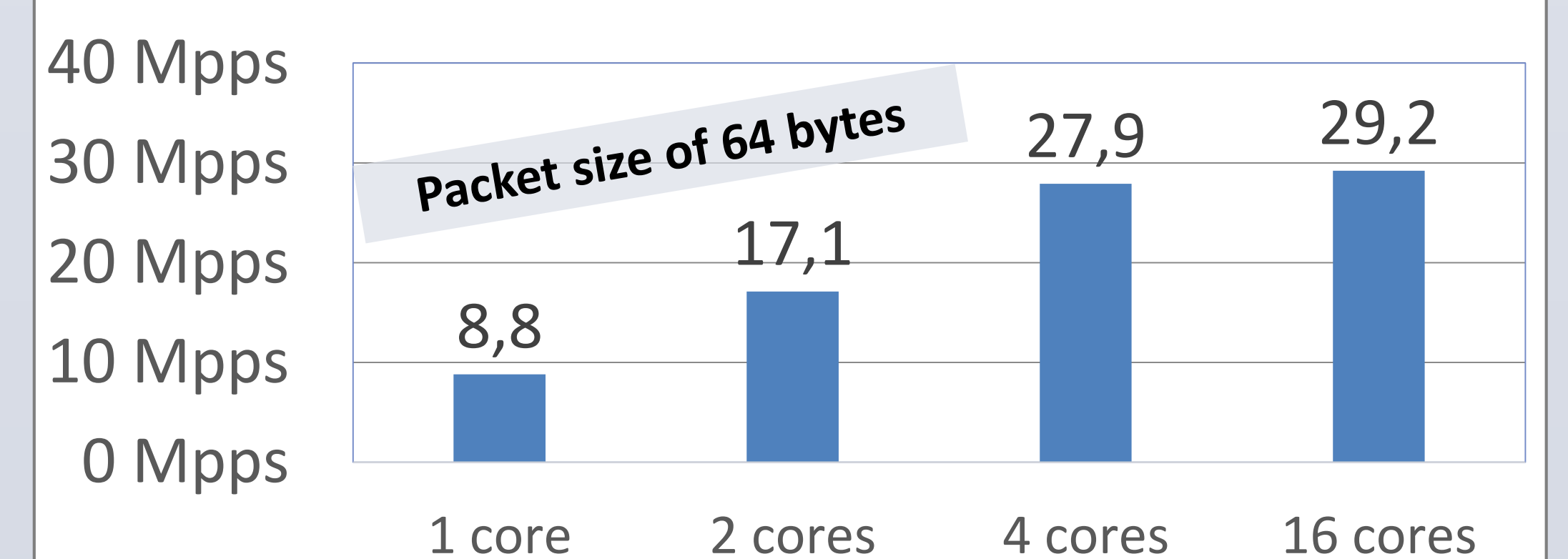
CONTACT

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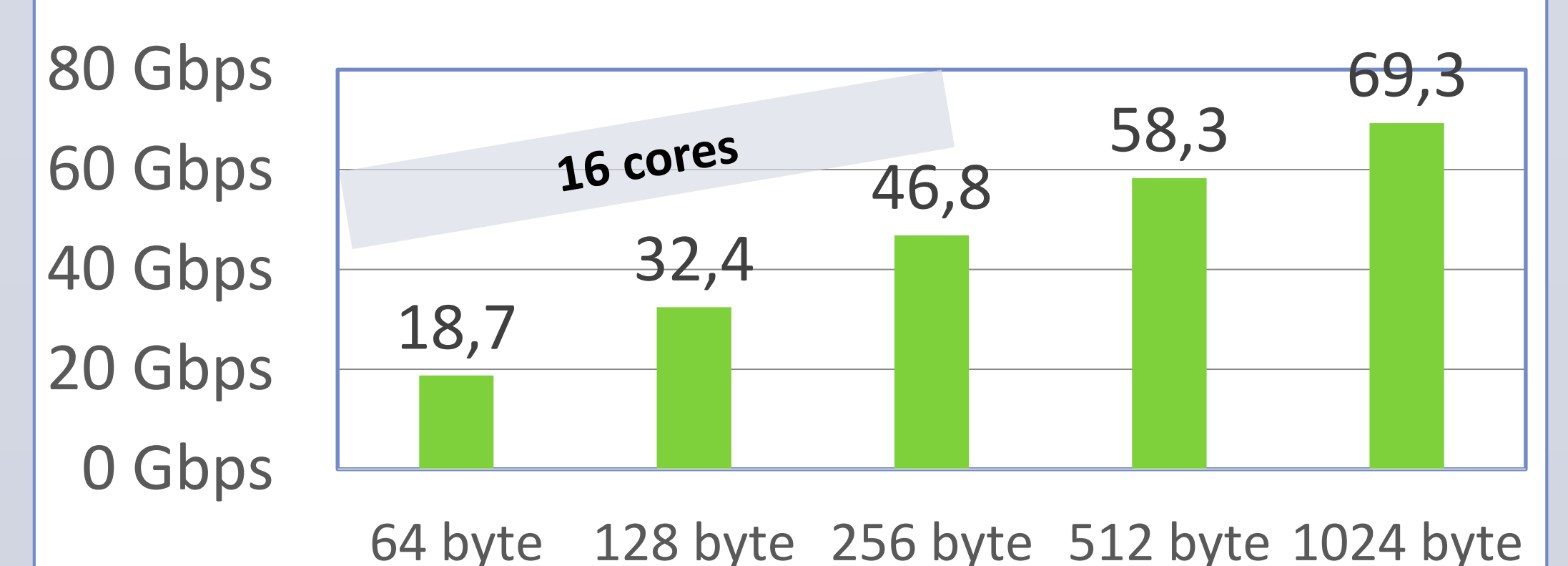
L2 RX rates 24 table entries



L2 RX rates 200 table entries



L2 RX rates 200 table entries



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